REMARKS

Claims 1, 3-9, 11-17, 19-25, and 27-31 are pending. Claims 1, 9, 17, and 25 are independent.

Applicant amended independent claim 1 to clarify that the queue entry includes a plurality of Buffer Descriptor Address (BDA) entries and that each BDA entry includes the address of one of a plurality of data buffer and the corresponding number of cells in that data buffer. Support for this clarification may be found, for example, in FIGS. 2A-2C, and on page 4, lines 3-18 of the originally filed application. Applicant similarly amended independent claims 9, 17, and 25. In addition, applicant also amended claim 7 to clarify that the queue count indicates the number of BDA entries included in the queue entry. Applicant similarly amended claims 15, 23, and 31. Support for this clarification may be found, for example, at page 6, lines 5-7 of the originally filed application.

The examiner rejected claims 1, 3-6, 8, 9, 11-14, 16, 17, 19-22, 24, 25, and 27-30 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,822,958 to Branth et al. in view of U.S. Patent No. 5,850,395 to Hauser et al. The examiner also rejected claims 7, 15, 23, and 31 under 35 U.S.C. §103(a) as being unpatentable over Branth and Hauser and further in view of U.S. Patent No. 6,320,861 to Adam et al.

Independent claim 1 describes a method of managing queue entries that includes the feature of "storing addresses corresponding to one of a plurality of data buffers having a corresponding number of cells in a first queue entry configured as a circular linked list comprising a plurality of Buffer Descriptor Address (BDA) entries, ... each of the plurality of BDA entries of the circular linked list includes one of the data buffer addresses and an associated cell count that indicates the corresponding number of cells contained in the corresponding data buffer." Applicant's independent claim 1 thus enables a more efficient storage management and processing (e.g., transmission) of data by using the queue entry recited in independent claim 1 to keep track and subsequently retrieve data stored in non-contiguous data buffers. Applicant's queue entry thus reduces the overhead that would otherwise be required to keep track and process individual data cells.

Branth, on the other hand, discloses an ATM switch for transmitting a multicast ATM cell (Abstract). Branth uses a data structure, shown in FIG. 6, in which a master entry 330 identifies the sequence of cells in memory that are to be multicast (i.e., transmitted to multiple destinations). Linked to the master entry are the multicast member entries that identify the connections on which multicast cells are to be transmitted (col. 8, lines 65-67). When a sequence of ATM cells, identified by the master entry, is to be transmitted, the ATM switch accesses each of the multicast members linked to the master entry to determine the target connection, and thus destination, to which that sequence of cells is to be transmitted. Thus, the multicast members linked to the master entry 330 do not store addresses of data buffers that are to be transmitted to a destination, but rather store connection information identifying multiple destinations. Moreover, since Branth multicast entries do not point or otherwise pertain to the actual data that is to be transmitted, those multicast entries do not include any information relating to the number of data cells. Accordingly, Branth does not disclose or suggest "storing addresses corresponding to one of a plurality of data buffers having a corresponding number of cells in a first queue entry configured as a circular linked list comprising a plurality of Buffer Descriptor Address (BDA) entries, ... each of the plurality of BDA entries of the circular linked list includes one of the data buffer addresses and an associated cell count that indicates the corresponding number of cells contained in the corresponding data buffer", as required by independent claim 1.

Hauser also fails to disclose applicant's queue entry as recited in independent claim 1. Specifically, Hauser discloses an ATM based service consolidation switch (Abstract). To transmit data, Hauser uses a queue implemented as a linked list of cells (FIG. 6, and col. 13, lines 1-13). A queue descriptor points to the first cell in the queue, and each cell in the linked lists points to the subsequent cell (col. 13, lines 1-13, and lines 44-65). Thus, unlike applicant's queue entry, Hauser's queues are linked lists of the actual data cells, and not queues comprising BDA entries that point to corresponding data buffers. Further, since cells in Hauser's queues point to subsequent individual cells rather than to data buffers, Hauser does not have keep track of the cell count in data buffers (there are no data buffers to keep track of). Accordingly, Hauser does not disclose or suggest "storing addresses corresponding to one of a plurality of data buffers having a corresponding number of cells in a first queue entry configured as a circular linked list comprising a plurality of Buffer Descriptor Address (BDA) entries, ... each of the plurality of

BDA entries of the circular linked list includes one of the data buffer addresses and an associated cell count that indicates the corresponding number of cells contained in the corresponding data buffer", as required by applicant's independent claim 1.

Since neither Branth nor Hauser discloses or suggests, alone or in combination, at least applicant's independent claim 1 feature of "storing addresses corresponding to one of a plurality of data buffers having a corresponding number of cells in a first queue entry configured as a circular linked list comprising a plurality of Buffer Descriptor Address (BDA) entries, ... each of the plurality of BDA entries of the circular linked list includes one of the data buffer addresses and an associated cell count that indicates the corresponding number of cells contained in the corresponding data buffer", applicant's independent claim 1 is thus patentable over the prior art cited by the examiner.

Claims 3-8 depend from independent claim 1 and are therefore patentable for at least the same reasons as independent claim 1.

Claims 9, 17, and 25 recite the feature of "store addresses corresponding to one of a plurality of data buffers having a corresponding number of cells in a first queue entry configured as a circular linked list comprising a plurality of Buffer Descriptor Address (BDA) entries, ... each of the plurality of BDA entries of the circular linked list includes one of the data buffer addresses and an associated cell count that indicates the corresponding number of cells contained in the corresponding data buffer", or similar language. For reasons similar to those provided with respect to independent claim 1, at least this feature is not disclosed in the art cited by the examiner. Accordingly, independent claims 9, 17 and 25 are patentable over the art cited by the examiner.

Claims 11-16 depend from independent claim 9 and are therefore patentable for at least the same reasons as independent claim 9. Claims 19-24 depend from independent claim 17 and are therefore patentable for at least the same reasons as independent claim 17. Claims 27-31 depend from independent claim 25 and are therefore patentable for at least the same reasons as independent claim 25.

Additionally, as noted, the examiner also rejected claims 7, 15, 23, and 31 under 35 U.S.C. §103(a) as being unpatentable over Branth and Hauser and further in view of Adam.

Claim 7 describes the feature of incrementing a queue count indicating the number of BDA entries included in the queue entry each time an address is linked to the first queue entry. Thus, as additional BDA entries are added to the queue entry, the queue count is incremented accordingly.

The examiner admits that "[t]he combination of Branth and Hauser discloses the elements of claims 1 and 3-5 as noted above but is silent regarding incrementing a queue count each time an address is linked to the first queue entry" (Office Action, page 8). The examiner, however, argues that "Adam discloses incrementing a queue count each time an address is linked to the first queue entry [col. 6, lines 34-45]".

Adam discloses a switch for an ATM communication system (Abstract). Adam describes that multicast cells (i.e., cells destined to multiple destinations) are placed on multiple multicast queues corresponding to the output ports on the ATM switch through which those multicast cells are to be sent (col. 6, lines 19-28). Adam further describes maintaining a count of the multicast cells placed on the multicast queues by incrementing the count by the number of queues a multicast cell has been written into when the multicast cell is enqueued (col. 6, lines 33-38). Thus, this count, as described by Adam, refers to the number of actual cells placed in output port multicast queues. This count, therefore, does not keep track of the number of Buffer Descriptor Address entries placed in a circular linked list corresponding to a queue entry. Indeed, Adam transmits data cells individually rather than transmitting data buffers, and therefore there are neither data buffers nor Buffer Descriptor Address entries to count. Accordingly, Adam does not disclose or suggest "incrementing a queue count indicating the number of BDA entries included in the queue entry each time an address is linked to the first queue entry", as required by applicant's claim 7.

Since none of the references cited by the examiner discloses or suggests, alone or in combination, at least the feature of "incrementing a queue count indicating the number of BDA entries included in the queue entry each time an address is linked to the first queue entry", claim 7 is patentable over the cited art.

Applicant's claims 15, 23, and 31 recite the feature of "increment a queue count indicating the number of BDA entries included in the queue entry each time an address is linked to the first queue entry", or similar language. For reasons similar to those provided with respect

to applicant's claim 7, at least this feature is not disclosed by the prior art cited by the examiner. Accordingly, claims 15, 23, and 31 are patentable over the art cited by the examiner.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

In view of the foregoing remarks, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

No fee is believed due. Please apply any charges to deposit account 06-1050, referencing attorney docket 10559-614001.

Respectfully submitted,

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